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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/631,952

07/30/2003

Edgardo F. Klass

P-9539

1785

7590

07/27/2004

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EXAMINER

NGUYEN, HAI L

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/631,952

**Applicant(s)**

KLASS, EDGARDO F.

**Examiner**

Hai L. Nguyen

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Drawings*

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
2. Figure 6 is objected to because the black box elements need textual labels. For example, element 611 should be labeled as --Logic Block-- as described in the specification. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes

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are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 6, 7, 9-12, 14, 16, 17, 19-22, 24, 26, 27, 29-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizuno et al. (US 6,229,360).

With regard to claims 1 and 11, Mizuno et al. discloses in Figs. 1-4 a clock skew tolerant clocking scheme, and the method of use thereof, comprising a data-stream (IN); a clock signal (CLK), the clock signal having a clock cycle, the clock signal comprising a plurality of clock pulses, each of the clock pulses of the plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between the clock pulse rising edge and the clock pulse falling edge; a first pulse signal (P1-1B), the first pulse signal being derived from the clock signal such that each of the first pulses of the plurality of first pulses corresponds to one of the clock pulses of the plurality of clock pulses and each of the first pulse rising edges of the first pulses are generated by a corresponding clock pulse rising edge of the corresponding one of the plurality of clock pulses, the first pulse width being less than fifty percent of the clock pulse width; a second pulse signal (P2-1B), the second pulse signal being derived from

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the clock signal such that each of the second pulses of the plurality of second pulses corresponds to one of the clock pulses of the plurality of clock pulses and each of the second pulse rising edges of the second pulses are generated by a corresponding clock pulse falling edge of the corresponding one of the plurality of clock pulses, the second pulse width being less than fifty percent of the clock pulse width; a first transparent pulse latch, the first pulse signal being operatively coupled to the first transparent pulse latch; a second transparent pulse latch, the second pulse signal being operatively coupled to the second transparent pulse latch wherein, for each clock pulse of the plurality of clock pulses of the clock signal there is a first pulse of the plurality of first pulses of the first pulse signal generated by a rising edge of the clock pulse and a corresponding second pulse of the plurality of second pulses of the second pulse signal generated by a falling edge of the clock pulse; further wherein, there is a frequency dependent separation window between a falling edge of the first pulse and rising edge of the corresponding second pulse such that race conditions are avoided.

With regard to claims 2, 4, 6, 7, 12, 14, 16, and 17; the references also meet the recited limitations in these claims (see column 8, line 36 through column 10, line 9).

With regard to claims 9, 10, 19, and 20; the first pulse signal is generated by a first local pulse generator (21-25 in instant Fig. 2) operatively coupled to the first transparent pulse latch (1 and 5); and the second pulse signal is generated by a second local pulse generator (21-24 in instant Fig. 3) operatively coupled to the second transparent pulse latch (3).

Claim 21 is similarly rejected; note the above discussion with regard to claims 1 and 11. Furthermore, the limitation "providing a plurality of pipeline stages, each of the

stages comprising combinational logic blocks” is also met by the reference (Fig. 1 of Mizuno et al.).

Claims 22, 24, 26, 27, 29, and 30 are similarly rejected; note the above discussion with regard to claims 2, 4, 6, 7, 12, 14, 16, 17, 19, and 20.

With regard to claims 31 and 32, Mizuno et al. discloses in Figs. 1-4 a clock skew tolerant clocking scheme comprising a data stream (IN); a clock signal (CLK), the clock signal having a clock cycle, the clock signal comprising a plurality of clock pulses; a first pulse signal (P1-1B), the first pulse signal being derived from the clock signal such that each of the first pulses of the plurality of first pulses corresponds to one of the clock pulses of the plurality of clock pulses and each of the first pulse rising edges of the first pulses are generated by a corresponding clock pulse falling edge of the corresponding one of the plurality of clock pulses, the first pulse width being less than fifty percent of the clock pulse width; a second pulse signal (P2-1B), the second pulse signal being derived from the clock signal such that each of the second pulses of the plurality of second pulses corresponds to one of the clock pulses of the plurality of clock pulses and each of the second pulse rising edges of the second pulses are generated by a corresponding clock pulse rising edge of the corresponding one of the plurality of clock pulses, the second pulse width being less than fifty percent of the clock pulse width; a first transparent pulse latch (1, 3), the first pulse signal being operatively coupled to the first transparent pulse latch; a second transparent pulse latch (5), the second pulse signal being operatively coupled to the second transparent pulse latch; wherein, for each clock pulse of the plurality of clock pulses of the clock signal there is a first pulse of the plurality of first pulses of the first pulse signal generated by a falling edge of the clock

pulse and a corresponding second pulse of the plurality of second pulses of the second pulse signal generated by a rising edge of the clock pulse; further wherein, there is a frequency dependent separation window between a falling edge of the first pulse and rising edge of the corresponding second pulse such that race conditions are avoided.

Claim 33 is similarly rejected; note the above discussion with regard to claims 31 and 32. Furthermore, the limitation "providing a plurality of pipeline stages, each of the stages comprising combinational logic blocks" is also met by the reference (Fig. 1 of Mizuno et al.).

Claims 34-36 are similarly rejected; note the above discussion with regard to claims 31 and 32. Furthermore, the limitation "providing a plurality of pipeline stages, each of the stages comprising combinational logic blocks", in claim 36, is also met by the reference (Fig. 1 of Mizuno et al.).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3, 5, 8, 13, 15, 18, 23, 25, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al.

With regard to claims 3, 5, and 8; the above discussed that the circuit, and the method of use thereof, of Mizuno et al. meets all of the claimed limitations except for the limitation that the first and second pulse widths are twenty percent of the clock cycle. It

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would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to set the first and second pulse widths at a desired width to meet the specific condition of the particular application. It has been held that discovering an optimum range or to optimally match to an application is obvious to the skilled artisan. See *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 13, 15, 18, 23, 25, and 28 are similarly rejected; note the above discussion with regard to claims 3, 5, and 8.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Makino (US 6,525,587) is cited as of interest because it discloses a semiconductor integrated circuit device including a clock synchronous type logical processing circuit.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.



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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN *HLN*  
July 18, 2004



TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800